CLAIMS

What is claimed is:

1. A method for determining failure rate and selecting a best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each said integrated circuit under a testing environment, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environment and a real time of a normal operating environment;

performing a simulating process, using a testing time function to simulate said failure rate testing time relation;

performing a transforming process, using said acceleration factor function to transform said testing time function into a real time function, wherein a knee point of said real time function corresponds to an operation time which is said best burn-in time; and

performing an integrating process, integrating said real time function through a calculating region to consult an accumulated failure rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

2. The method of claim 1, wherein said failure rate testing time relation is divided into three periods in according to value of said testing time, said three periods are a infant mortality period, a normal life period and a wear out period.

3. The method of claim 1, wherein said acceleration factor function is a constant.

4. The method of claim 1, wherein said acceleration factor function is a linear function.

5. The method of claim 1, wherein said acceleration factor function is a nonlinear function.

6. The method of claim 1, wherein said testing time function is an exponent function.

7. The method of claim 1, wherein said testing time function is a polynomial of said testing time.

8. The method of claim 1, wherein said testing time function is $y=at^b$, wherein a and b are two variables, y is said failure rate and t is said testing time.

9. The method of claim 1, wherein said simulating process is adjusted to let a last square error between said failure rate testing time relation and said testing time function is minimized.

10. The method of claim 1, wherein said simulating process is adjusted to let an error between said failure rate testing time relation and said testing time function is minimized.

11. The method of claim 2, wherein said integrating process is stopped while said testing time in which is corresponds by said testing time is located in said wear out period.

12. A method for determining failure rate and selecting best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each said integrated circuit under a testing environment, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environment and a real time of a normal operating environment;

performing a transforming process, using said acceleration factor function to transform said failure rate testing time function into a failure rate real time function,

performing a simulating process, using a real time function to simulate said failure rate real time relation, wherein a knee point of said real time function corresponds to an operation time which is a best burn-in time for testing said integrated circuits; and

performing an integrating process, integrating said real time function through a calculating region to consult an accumulated failure rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

13. The method of claim 12, wherein said failure rate testing time relation is divided into three periods: an infant mortality period, a

normal life period and a wear out period.

14. The method of claim 12, wherein said acceleration factor function is chosen from the group consisting of: constant, linear function and nonlinear function.

15. The method of claim 12, wherein said testing time function is $y=at^b$, wherein a and b are two variables, y is said failure rate and t is said real time.

16. The method of claim 12, wherein said simulating process is adjusted to let a last square error between said failure rate real time relation and said real time function is minimized.

17. The method of claim 12, wherein said simulating process is adjusted to let an error between said failure rate real time relation and said real time function is minimized.

18. The method of claim 13, wherein said integrating process is stopped while said testing time in which is corresponds by said testing time is located in said wear out period.

19. A method for determining failure rate and selecting best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein the life-time of each said integrated circuit is measured under a testing environment and then a failure rate testing time relation is established in accordance

with a plurality of testing records, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environments and a real time of a normal operating environment;

performing a simulating process, using a testing time polynomial of said testing time to simulate said failure rate testing time relation;

performing an optimizating process, part of said testing records are deleted and said corresponding processes are performed again while more than one said integrated circuits are failed before a specific testing time in which is corresponding to a knee point of said testing time polynomial, and said specific testing time is a best testing time of said integrated circuits while only one of said integrated circuits is failed before said specific testing time;

performing a transforming process, using said acceleration factor function to transform said specific testing time into a specific real time and also transform said testing time polynomial into a real time polynomial, wherein said specific real time is a best burn-in time for testing said integrated circuits; and

performing an integrating process, integrating said real time function through a calculating region to consult an accumulated failure rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

20. The method of claim 19, wherein said integrating process is stopped while said testing time in which is corresponds by said testing time is located in said wear out period.